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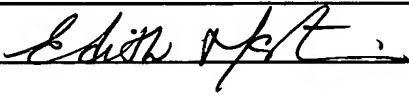
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

P17171

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on August 14, 2006

Signature 

Typed or printed name Edith Martin

Application Number

10/689,998

Filed

October 21, 2003

First Named Inventor

Kooi, Chee Choong

Art Unit

2841

Examiner

Carpio, Ivan Hernan

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.


I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record. 41,339
Registration number

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____


Signature

Nandu A. Talwalkar
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Telephone number

August 14, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: KOOI et al.

Application No.: 10/689,998

Filing Date: 10/21/2003

For: INTEGRATED CIRCUIT
PACKAGING SYSTEM

) Group Art Unit: 2841
)
) Examiner: Ivan H. Carpio
)
) **Reason(s) for Requesting a Pre-Appeal**
) **Brief Review**
)
) Attorney Docket No.: P17171
)
) **PTO Customer Number 28062**
) Buckley, Maschoff & Talwalkar LLC
) Attorneys for Intel Corporation
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CERTIFICATE OF MAILING UNDER 37 CFR 1.8

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Dated: August 14, 2006

By:


Edith Martin

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit arguments in support of the Pre-Appeal Brief Request for Review filed herewith.

Arguments begin on page 2 of this paper.

ARGUMENTS

Applicants raise the following arguments as evidence of clear error in the outstanding final rejection of independent Claims 1, 6, 11 and 16.

Claims 1 and 16

Independent Claim 1 relates to an apparatus including an integrated circuit die, an integrated circuit package coupled to a first face of the integrated circuit die, and mold compound in contact with the integrated circuit die and the integrated circuit package (emphasis added). The mold compound includes a face substantially coplanar with a second face of the integrated circuit die, and the apparatus further includes an overlayer coupled to the face of the mold compound and to the second face of the integrated circuit die. The overlayer may, in some embodiments, reduce a tendency of the mold compound to delaminate from the die and/or the integrated circuit package.

The art of record is not seen to disclose or to suggest at least mold compound in contact with an integrated circuit die and an integrated circuit package, wherein the mold compound includes a face substantially coplanar with a second face of the integrated circuit die, and an overlayer coupled to the face of the mold compound and to the second face of the integrated circuit die.

For example, FIG. 9 of Cobbley illustrates array 150 including semiconductor dice 120 and dielectric filler material 136 that are coupled to flexible substrate 130 as shown. Redistribution lines 140 are formed on outer surface 138 of material 136. The Office Action indicates that the "integrated circuit package" of Claims 1 and 16 reads on distribution lines 140. Applicants respectfully disagree.

As described at col. 8, lines 8 through 63 of Cobbley, redistribution lines 140 are conductive traces extending from exposed end portions 128 of conductive elements 126 to various predetermined locations on outer surface 138. Redistribution lines 140 may be formed thereon using "any known method for patterning a thin layer of material" (see col. 8, lines 37 and

38), or "may be preformed on a flexible dielectric tape or film carrier" (see col. 8, lines 45 and 46).

M.P.E.P §2111.01 indicates that the words of a claim must be interpreted broadly but consistently with their "plain meaning". The phrase "plain meaning" refers to the ordinary and customary meaning given to the words by those of ordinary skill in the art. Applicants submit that no interpretation of the words "integrated circuit package" can reasonably encompass redistribution lines 140, which merely consist of a thin layer of conductive traces.

The remaining art of record has been reviewed and is not seen to remedy the foregoing deficiencies in Cobbley. Specifically, Bhattacharyya is not seen to add any relevant description that, alone or in combination with Cobbley, would disclose or suggest mold compound in contact with an integrated circuit die and an integrated circuit package, wherein the mold compound includes a face substantially coplanar with a second face of the integrated circuit die, and an overlayer coupled to the face of the mold compound and to the second face of the integrated circuit die.

Amended independent Claim 1 is therefore believed to be in condition for allowance. Amended independent Claim 16 relates to a system including the elements of amended Claim 1 and is believed to be allowable for at least the foregoing reasons.

Claim 6

Independent Claim 6 relates to an apparatus including an integrated circuit package substrate and a plurality of integrated circuit die, wherein a first face of each of the plurality of integrated circuit die is attached to the integrated circuit package substrate. The apparatus also includes mold compound in contact with the plurality of integrated circuit die and the integrated circuit package substrate, the mold compound comprising a face substantially coplanar with a second face of each of the plurality of integrated circuit die, and an overlayer coupled to the face of the mold compound and to the second face of each of the plurality of integrated circuit die.

As described above, the cited art is not seen to disclose or suggest an integrated circuit package substrate arranged as claimed in Claim 6. Specifically, neither Cobbley nor Bhattacharyya, taken alone or in any permissible combination, is seen to disclose or to suggest

mold compound in contact with an integrated circuit die and an integrated circuit package substrate, wherein the mold compound includes a face substantially coplanar with a second face of each of a plurality of integrated circuit die, and an overlayer coupled to the face of the mold compound and to the second face of each of the plurality of integrated circuit die.

Amended Claim 6 and its respective dependent Claims 7 through 10 are therefore believed to be allowable.

Claim 11

Claim 11 concerns a method that includes including placing an overlayer in contact with a face of mold compound and a first face of an integrated circuit die substantially coplanar with the face of the mold compound. According to the method, a second face of the integrated circuit die is coupled to an integrated circuit package, and the mold compound is in contact with the integrated circuit die and the integrated circuit package.

Nowhere does Cobbley disclose an integrated circuit package. Accordingly, Cobbley cannot be seen to disclose or to suggest coupling a second face of an integrated circuit die to an integrated circuit package, and/or mold compound in contact with the integrated circuit die and the integrated circuit package. Amended independent Claim 11 and dependent Claims 12 through 15 are therefore believed to be in condition for allowance.

Withdrawal of the outstanding final rejection under 35 U.S.C. §102 is therefore respectfully requested.

CONCLUSION

For at least the reasons given above, it is submitted that the final rejection of the application is improper and should be withdrawn. If any questions arise regarding the application or any of the cited references, or if the panel has suggestions for expediting allowance of the application, the panel is kindly invited to contact the undersigned via telephone at (203) 972-0049.

Respectfully submitted,



August 14, 2006
Date

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